Project 1: 433 MHz Low Noise Amplifier Design Using the BFU520 Transistor

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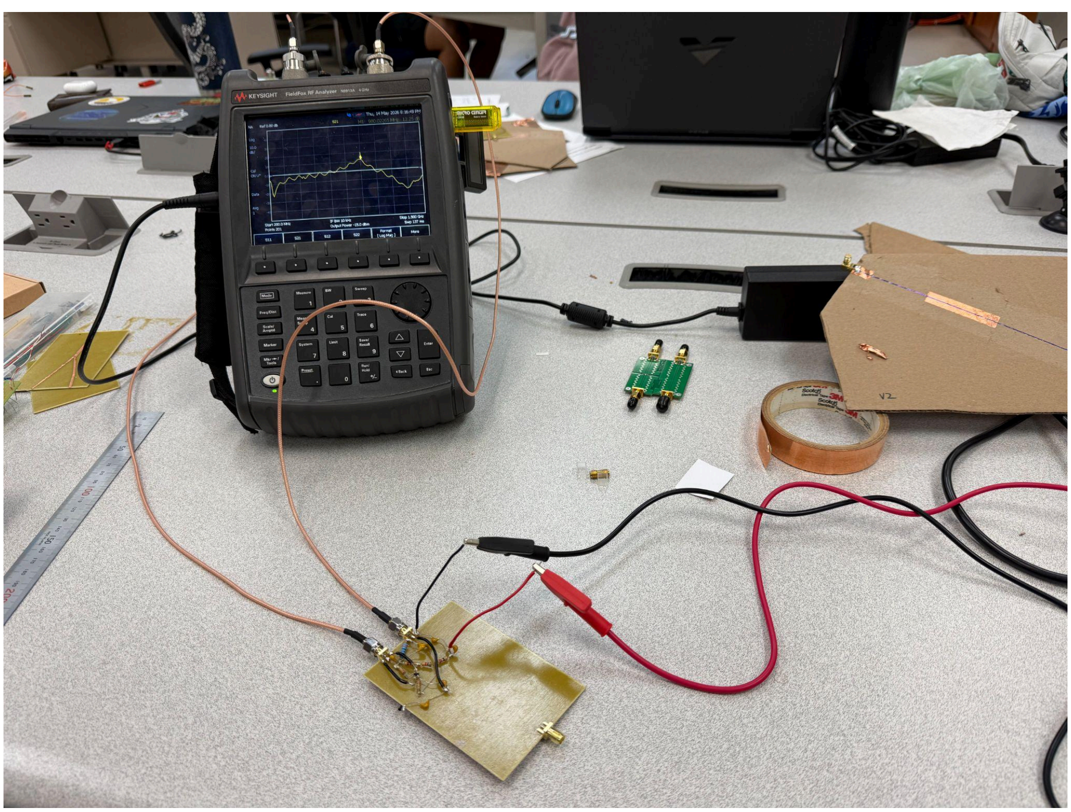
EE444

14 May 2026



Introduction

The objective of this project was to design, simulate, implement, and measure a low noise amplifier (LNA) operating within the 433 MHz ISM band using a BFU520 transistor. The amplifier was designed in ADS using microstrip transmission line techniques and lumped matching components before being physically implemented and measured using a Vector Network Analyzer (VNA).

The project required the measurement of the transistor Q-point as well as the amplifier S-parameters over the frequency range from 200 MHz to 600 MHz. The amplifier was initially constructed on a standard protoboard; however, the first implementation did not achieve the expected gain performance. A second implementation using an FR4 substrate with a continuous copper ground plane was then constructed, which significantly improved amplifier operation and stability.

The final fabricated amplifier demonstrated proper RF amplification behavior, although the resonant frequency shifted higher than the intended 433 MHz center frequency due to practical fabrication parasitics and layout effects.

Design and Simulation

The LNA was designed using the BFU520 transistor operating from a 3.6 V DC supply. The design utilized transmission line matching sections together with lumped inductors and capacitors to achieve gain and impedance matching near 433 MHz.

The ADS simulation included:

- S-parameter simulation from 200 MHz to 600 MHz
- DC bias analysis
- Microstrip substrate modeling
- Input and output matching optimization

The transistor bias network was adjusted to establish the desired Q-point while maintaining stable amplifier operation.

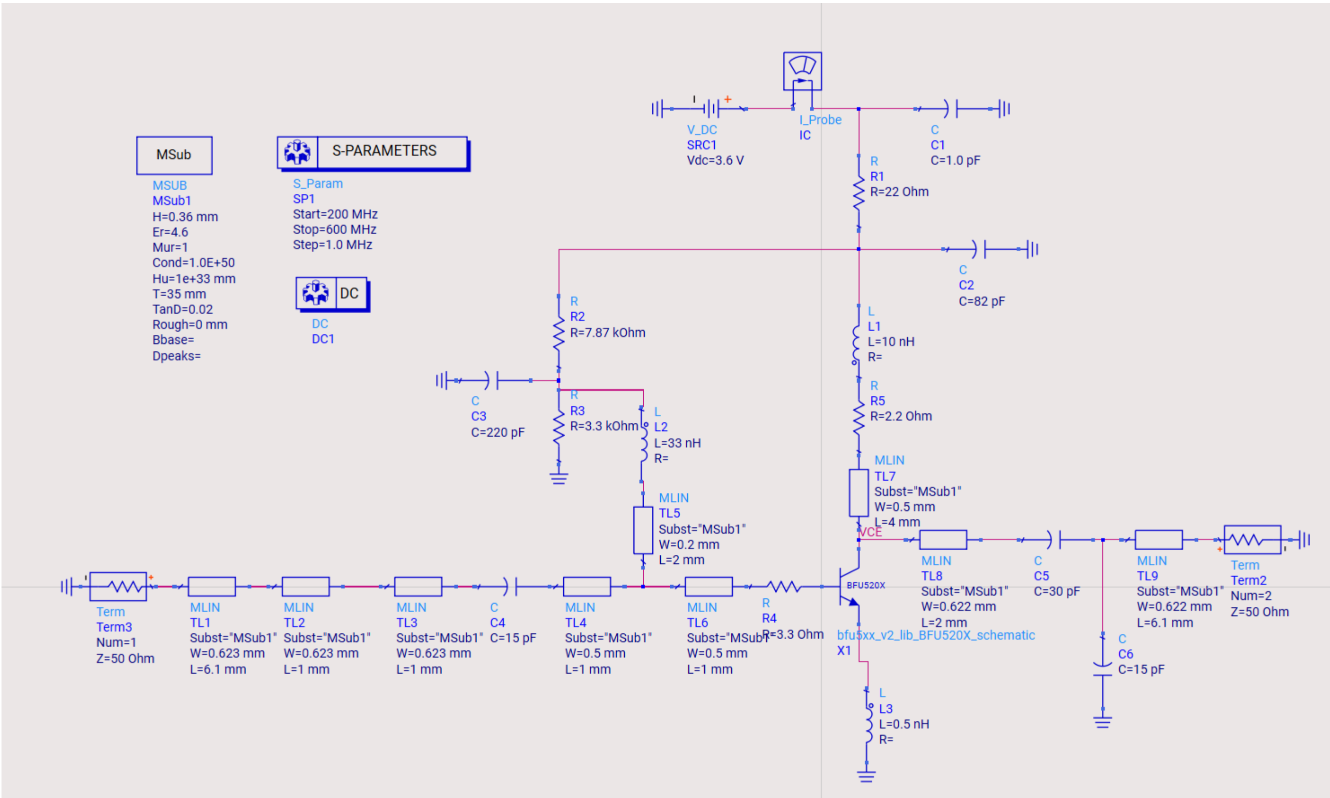


Figure 1. ADS schematic and simulation setup for the 433 MHz BFU520 low noise amplifier.

Simulation Results

After optimization, the ADS simulation produced approximately 20 dB of gain near the target frequency of 433 MHz.

The simulated S21 response showed:

- Forward gain ≈ 20.03 dB at 433 MHz

The simulated S11 response showed:

- Input return loss ≈ −4.71 dB at 433 MHz

The simulated S22 response showed:

- Output return loss ≈ −21.24 dB at 433 MHz

The simulated reverse isolation S12 showed:

- Reverse isolation ≈ −27.86 dB at 433 MHz

The DC operating point simulation produced:

- Collector current ≈ 7 mA
- Collector-emitter voltage ≈ 3.43 V

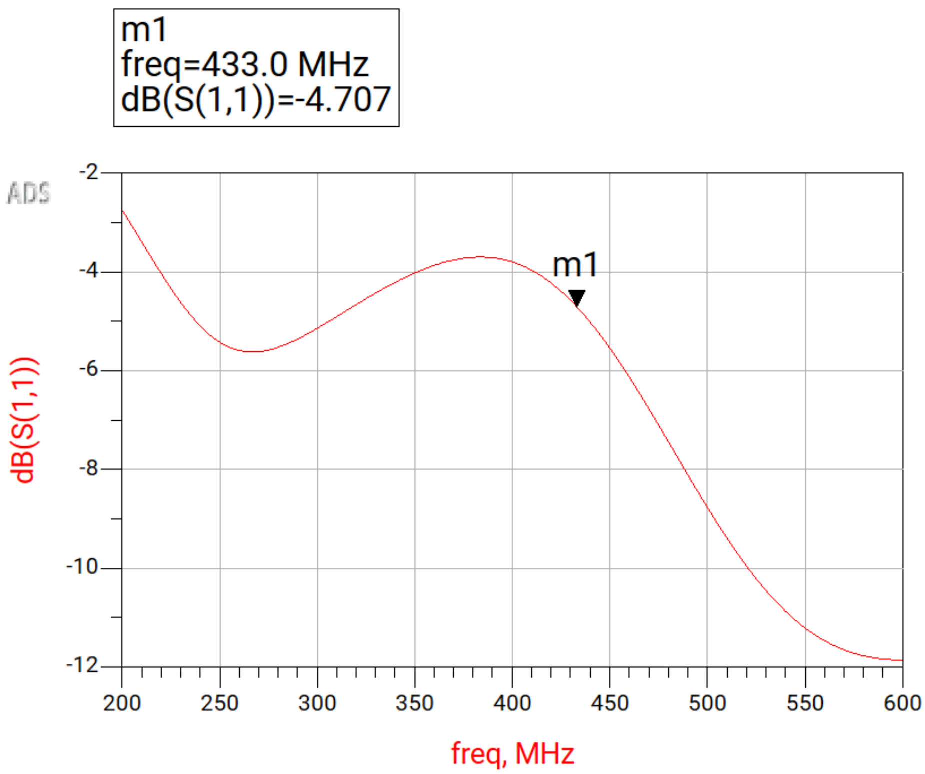


Figure 2. Simulated S11 response of the BFU520 LNA showing the input return loss near 433 MHz.

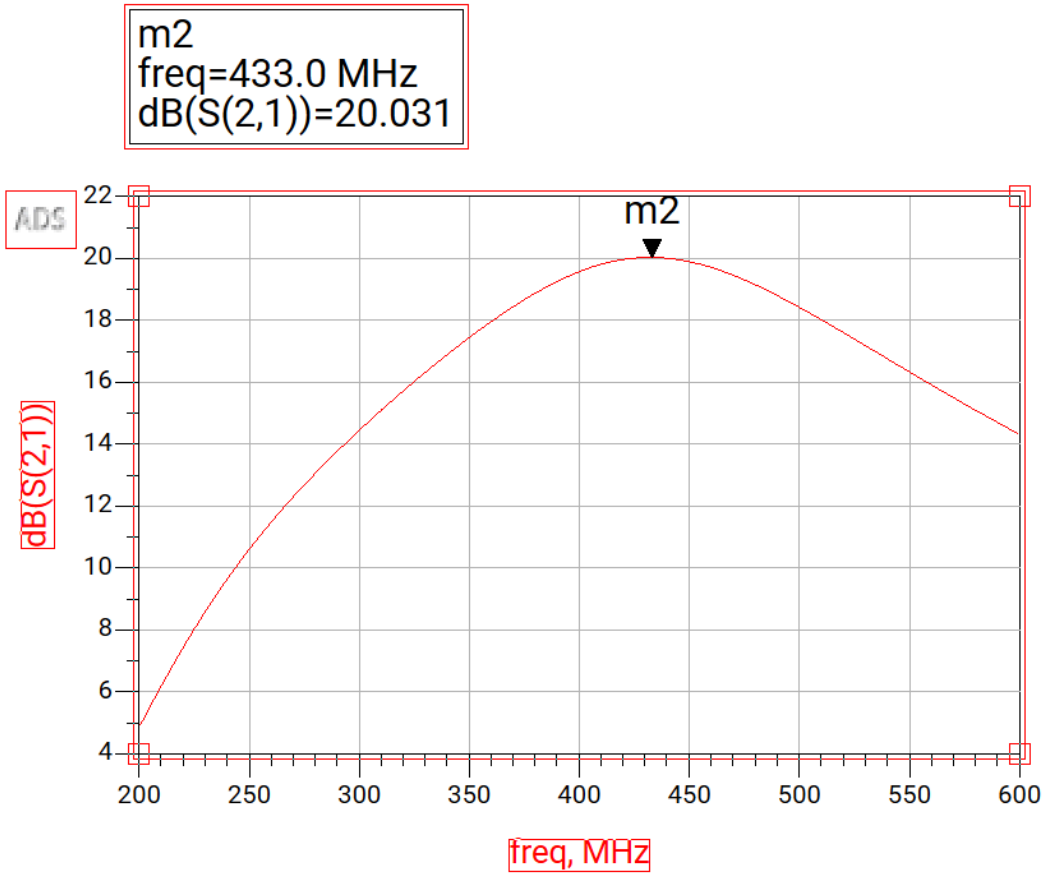


Figure 3. Simulated S21 response of the BFU520 LNA showing approximately 20 dB gain at 433 MHz.

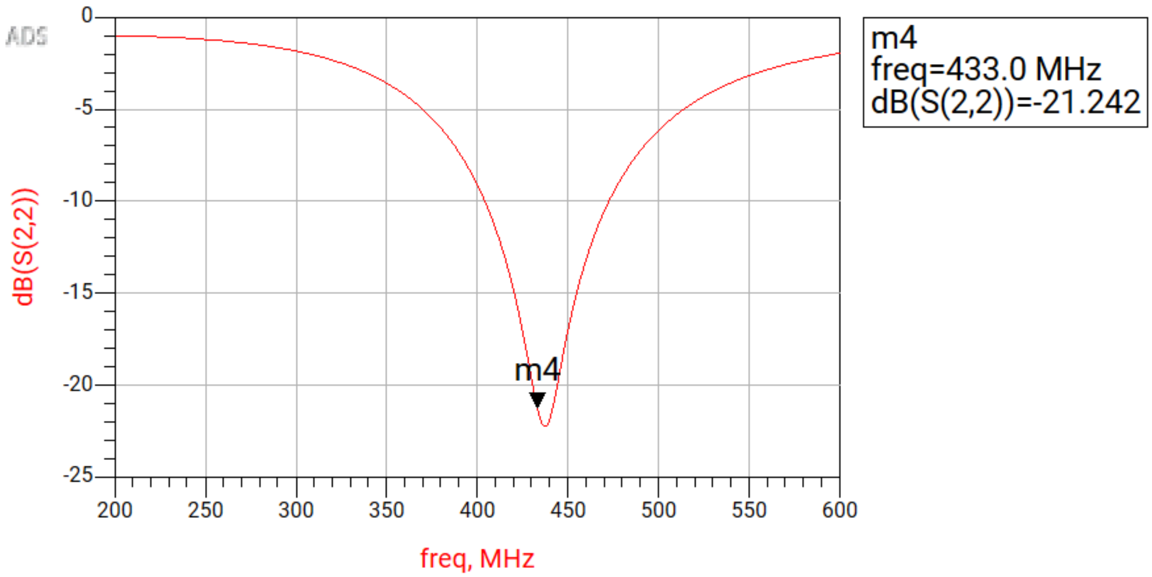


Figure 4. Simulated S22 response of the BFU520 LNA showing the output return loss characteristics.

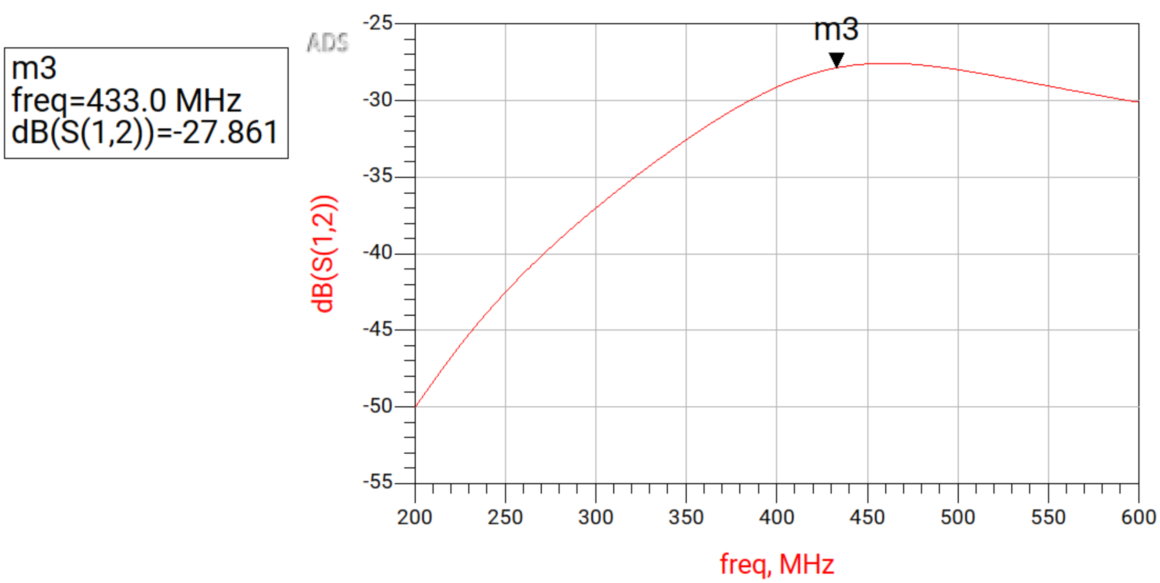


Figure 5. Simulated S12 response of the BFU520 LNA showing reverse isolation.

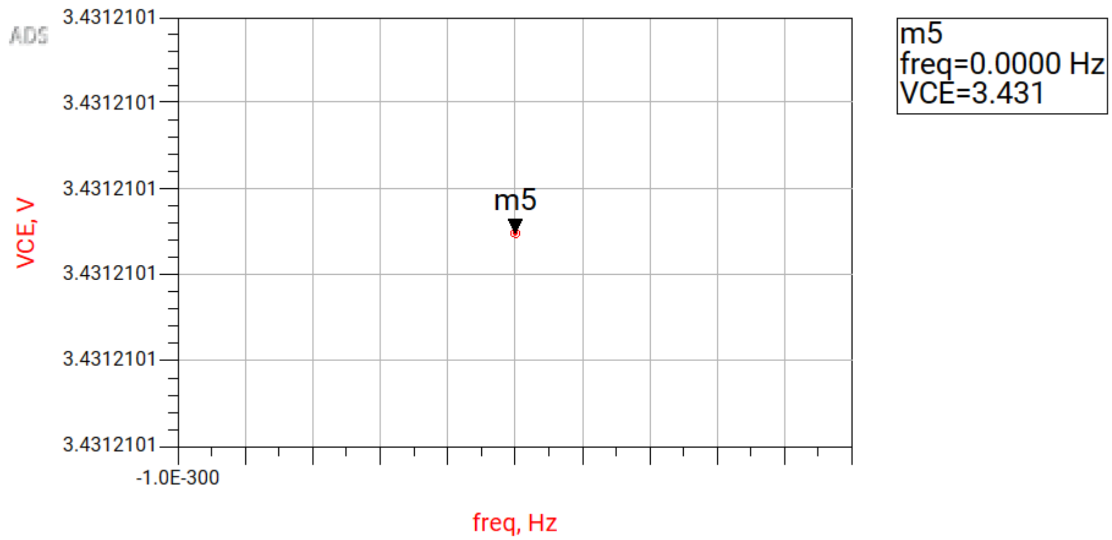


Figure 6. Simulated transistor Q-point showing collector-emitter voltage.

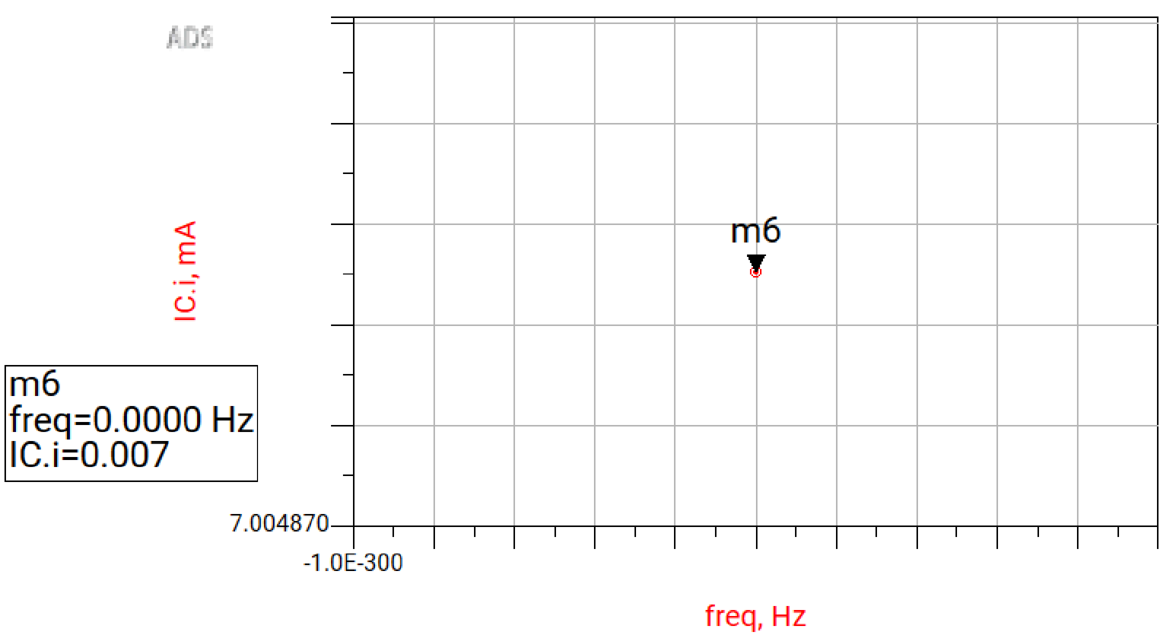


Figure 7. Simulated transistor Q-point showing collector current.

Initial Prototype Implementation

The first amplifier prototype was constructed using a standard protoboard with discrete through-hole components and SMA connectors. The amplifier was assembled using the ADS schematic as a reference and manually soldered together.

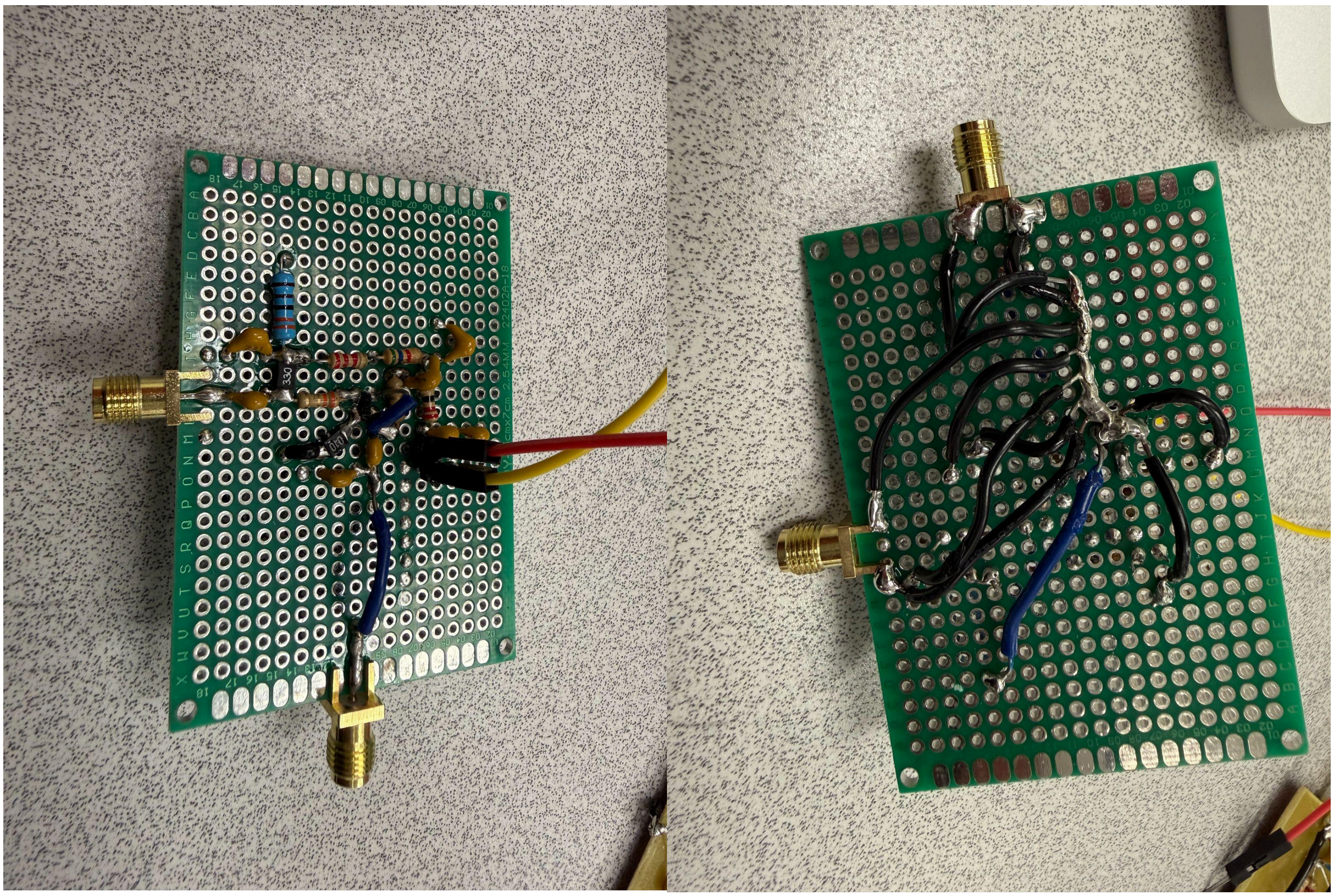


Figure 8. Initial protoboard implementation of the BFU520 low noise amplifier.

Although the amplifier was able to bias correctly, the measured gain performance was significantly lower than expected. The measured gain was approximately 1 dB while the return loss remained near −17 dB.

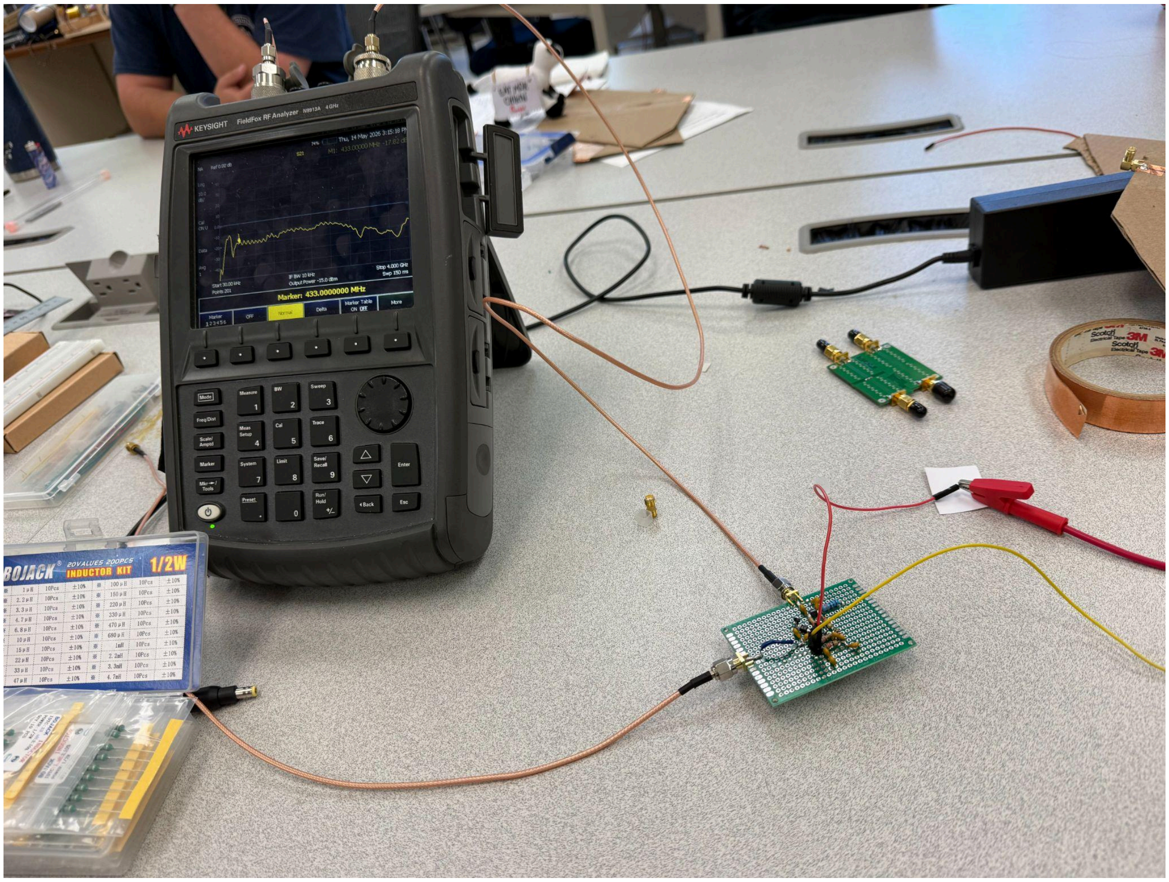


Figure 9. Measurement setup of the initial protoboard implementation using the Keysight FieldFox network analyzer.

The poor gain performance was likely caused by excessive parasitic inductance, lack of a continuous ground plane, long wiring paths, and unwanted coupling effects associated with the protoboard construction method. At UHF frequencies near 433 MHz, layout and grounding become critical factors in amplifier performance.

FR4 Ground Plane Redesign

After observing the limitations of the initial protoboard implementation, the amplifier was redesigned using an FR4 substrate with a continuous copper ground plane on the bottom side of the board.

The SMA connectors were directly soldered to the copper plane, and the amplifier components were mounted with significantly shorter lead lengths to reduce parasitic inductance and improve grounding.

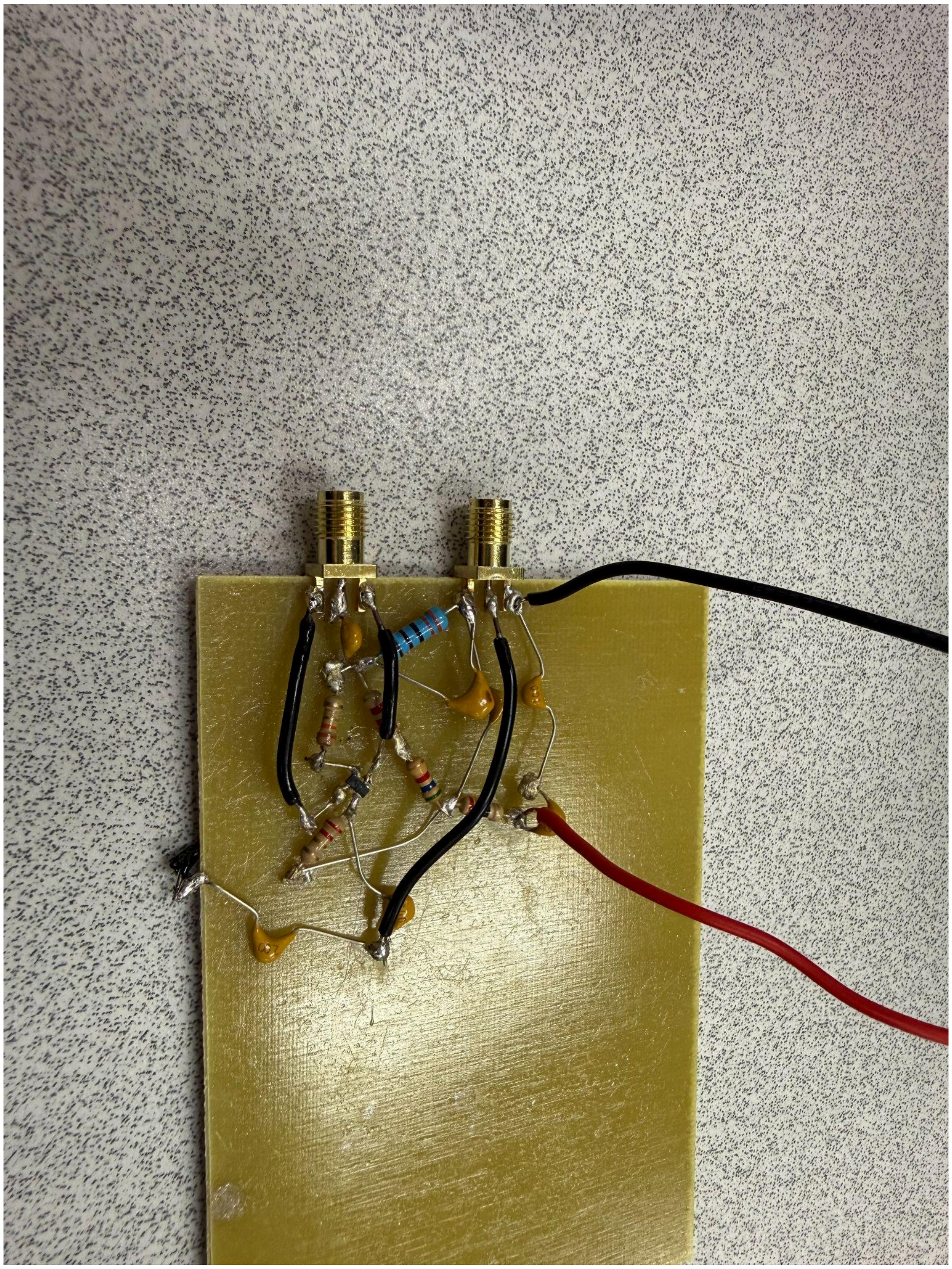


Figure 10. Final FR4 implementation of the BFU520 low noise amplifier.

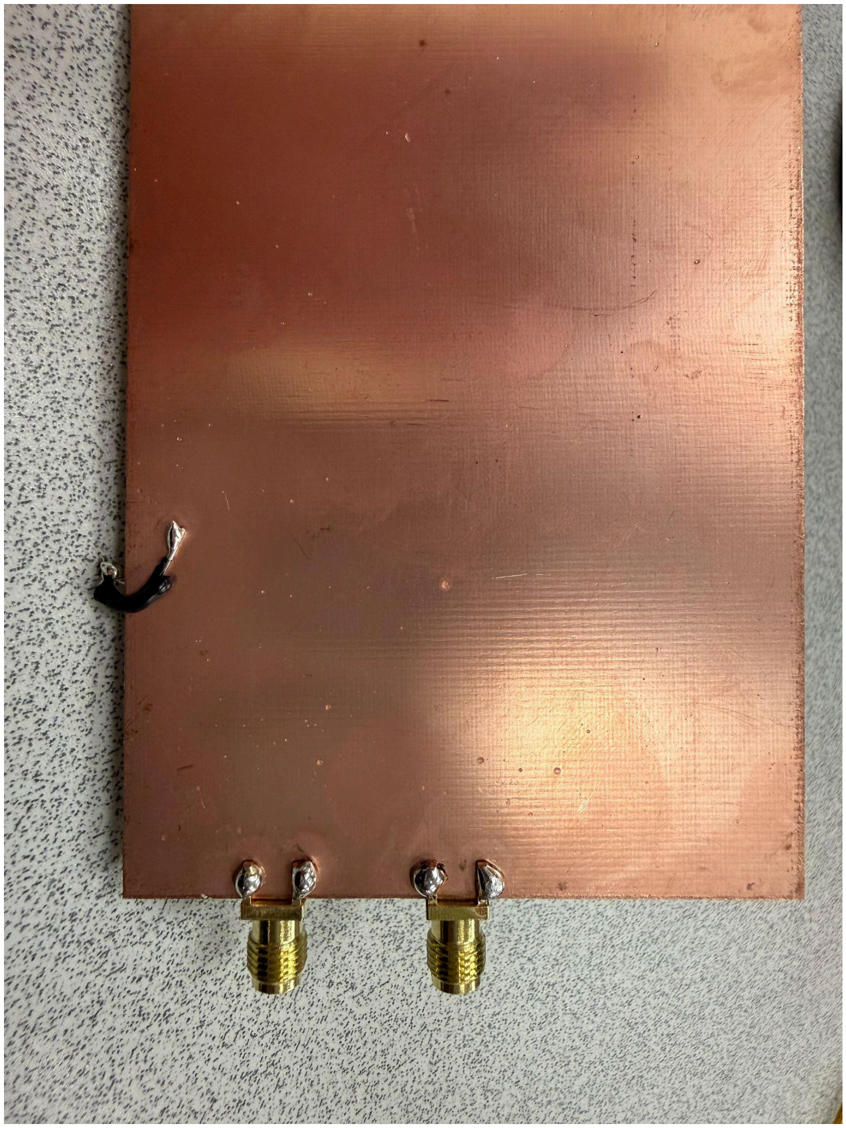


Figure 11. Copper ground plane used on the underside of the FR4 amplifier board.

The improved grounding and reduced parasitic effects significantly improved amplifier operation and stability compared to the original protoboard implementation.

Measurement Results

Measurements were performed using a Keysight FieldFox Network Analyzer over a frequency range extending beyond the original 433 MHz target frequency.

The measured amplifier response showed that the amplifier resonated closer to approximately 980 MHz instead of 433 MHz. Despite the frequency shift, the amplifier demonstrated proper RF amplification behavior and stable operation.

The measured S21 response showed:

- Forward gain ≈ 12.06 dB at approximately 980 MHz

The measured S11 response showed:

- Input return loss ≈ −16.42 dB at approximately 980 MHz

The measured S22 response showed:

- Output return loss ≈ −6.31 dB at approximately 980 MHz

The measured S12 response showed:

- Reverse isolation ≈ −22.45 dB at approximately 980 MHz

The measured transistor Q-point was approximately:

- Collector current ≈ 10 mA

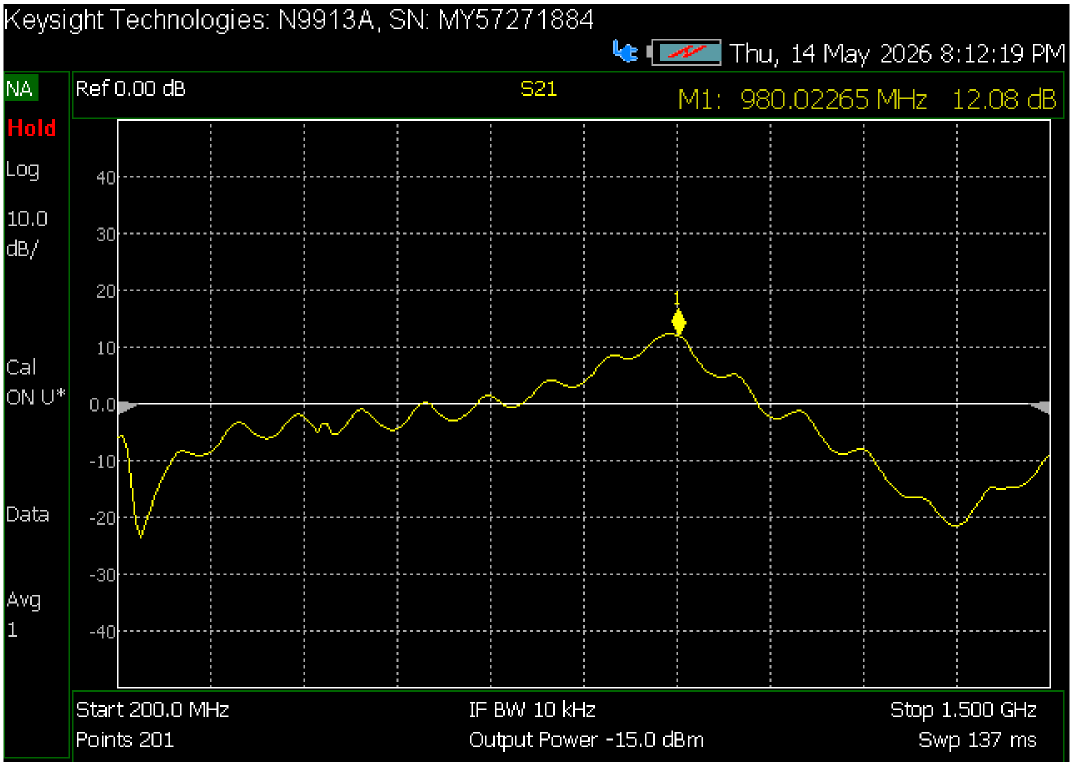


Figure 12. Measured S21 response of the fabricated FR4 amplifier showing approximately 12 dB gain near 980 MHz.

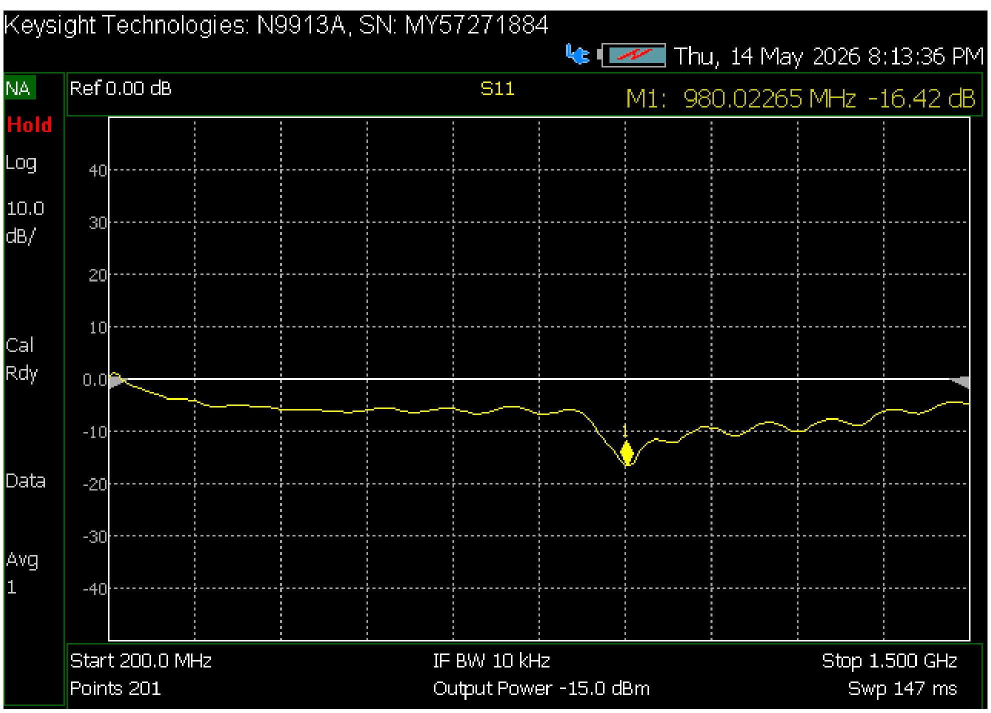


Figure 13. Measured S11 response of the fabricated FR4 amplifier.

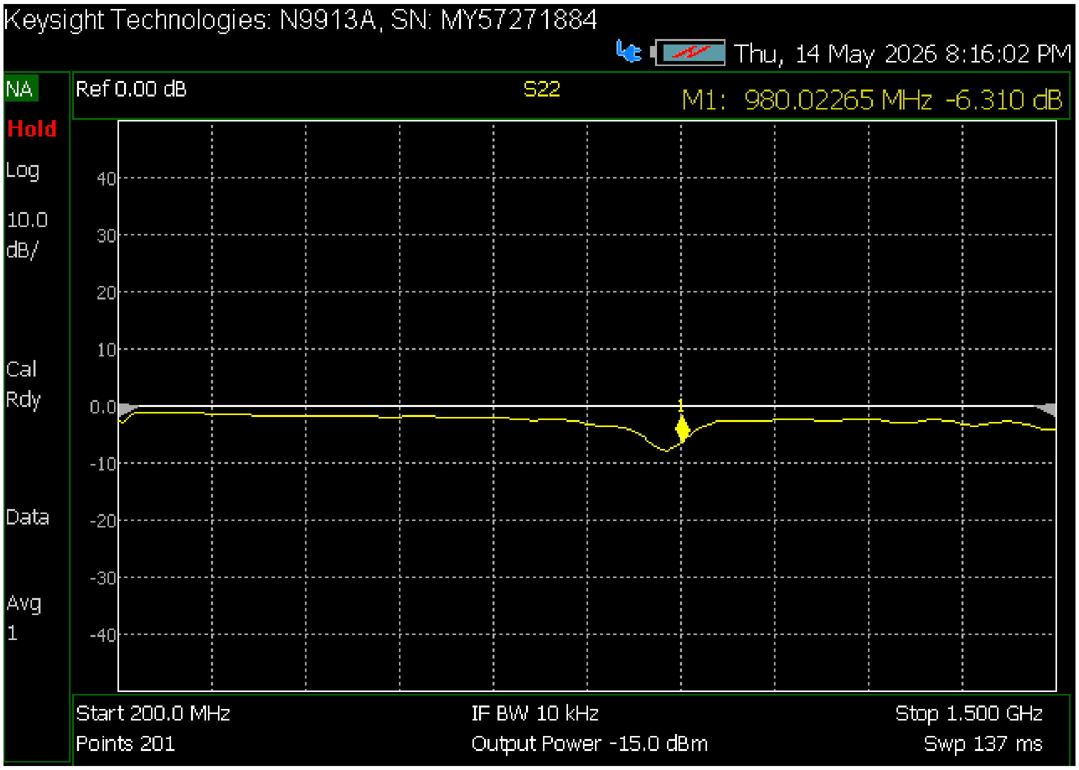


Figure 14. Measured S22 response of the fabricated FR4 amplifier.

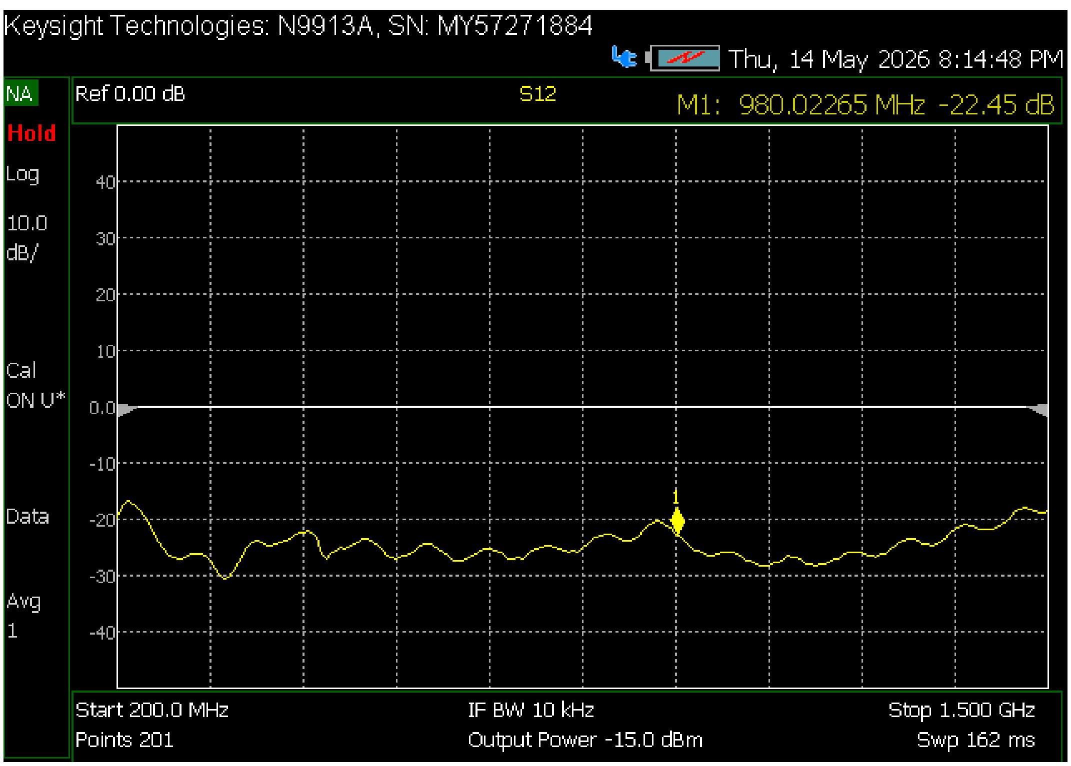


Figure 15. Measured S12 response of the fabricated FR4 amplifier.

Comparison of Simulated and Measured Results

Table 1 compares the ADS simulated performance with the measured performance of the fabricated amplifier.

Table 1. Comparison of simulated and measured BFU520 LNA performance

Parameter	ADS Simulation	Measured Result
Intended Center Frequency	433 MHz	~980 MHz
S21 Gain	20.03 dB	12.06 dB
S11 Return Loss	−4.71 dB	−16.42 dB
S22 Return Loss	−21.24 dB	−6.31 dB
S12 Reverse Isolation	−27.86 dB	−22.45 dB
Collector Current	7 mA	10 mA
Supply Voltage	3.6 V	3.6 V

The measured results differed from the ADS simulation primarily due to practical fabrication effects and layout parasitics associated with hand-built RF construction.

Discussion

The project demonstrated the strong sensitivity of RF amplifier performance to physical layout, grounding, and parasitic effects. The initial protoboard implementation produced very low gain despite maintaining acceptable return loss characteristics. This indicated that the amplifier topology itself was functioning, but the RF layout was preventing proper amplification.

One of the largest improvements came from redesigning the amplifier using an FR4 substrate with a continuous copper ground plane. The improved grounding significantly reduced parasitic inductance and improved return current paths, allowing the amplifier to operate much more effectively.

Although the final amplifier resonated near 980 MHz instead of the intended 433 MHz frequency, the amplifier still demonstrated proper low noise amplifier behavior with significant gain and acceptable stability. The frequency shift was most likely caused by practical differences between the ADS simulation and the physical implementation.

Several factors contributed to the frequency shift, including:

- Hand-built inductors differing from ideal values
- Shorter effective transmission line lengths
- Reduced parasitic capacitance
- Variations in FR4 dielectric properties
- Lead inductance and component placement variations

Additionally, the ADS simulation assumed ideal transmission line geometries and ideal lumped components, while the fabricated amplifier contained unavoidable parasitic effects introduced by solder joints, wiring, SMA connector transitions, and manual assembly.

Despite these differences, the project successfully demonstrated the practical implementation of a BFU520 low noise amplifier and highlighted the importance of RF grounding and layout techniques in UHF amplifier design.

Conclusion

A BFU520 low noise amplifier was successfully designed, simulated, fabricated, and measured using ADS and practical RF construction techniques.

The initial protoboard implementation demonstrated poor gain performance due to grounding and parasitic limitations. A second implementation using an FR4 substrate with a continuous copper ground plane significantly improved amplifier performance and stability.

Although the final amplifier resonated closer to 980 MHz instead of the intended 433 MHz center frequency, the fabricated amplifier demonstrated approximately 12 dB of gain together with acceptable return loss and reverse isolation characteristics. The project successfully demonstrated practical RF amplifier operation while also highlighting the major effects of layout parasitics and grounding on high-frequency circuit behavior.

Future improvements could include fabricating the amplifier using a professionally manufactured PCB, improving transmission line accuracy, using tighter tolerance lumped components, and further tuning the matching network to shift the resonant frequency closer to 433 MHz.